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Kartikeya Mayaram Un-Ku Moon

Spacecrafts experience radiation in the course of their operation and all electronic equipment on board these spacecrafts has to be designed to withstand the effects of this radiation. This thesis describes the effects of total ionization dose (TID) and single event transients (SET) in phase-locked loops - an important circuit block for communication circuits and clock generation.

The design of a digital phase-locked loop made tolerant to SET through redundancy and error correction techniques has been described. Digital phase-locked loops can also incorporate self-calibration techniques to compensate for the effects of TID. A linear analysis is presented for the design of digital phase-locked loops. This digital phase-locked loop was fabricated in the Honeywell 0.35μm SOI CMOS process.

Design Techniques for Radiation Hardened Phase-Locked Loops

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Anantha Nag Nemmani

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14. ABSTRACT

Spacecrafts experience radiation in the course of their operation and all electronic equipment on board these spacecrafts has to be designed to withstand the effects of this radiation. This thesis describes the e ects of total ionization dose (TID) and single event transients (SET) in phase-locked loops - an important circuit block for communication circuits and clock generation. The design of a digital phase-locked loop made tolerant to SET through redundancy and error correction techniques has been described. Digital phaselocked loops can also incorporate self-calibration techniques to compensate for the effects of TID. A linear analysis is presented for the design of digital phase-locked loops. This digital phase-locked loop was fabricated in the Honeywell 0.35 m SOI CMOS process.

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1. INTRODUCTION

1.1. Motivation

Space exploration provides us with valuable information about the universe. Progress in this field is contingent upon understanding and solving a number of issues. Radiation experienced by aircraft in the outer space is one of them. The various radioactive processes occurring in the cosmos, especially the sun are a source of radiation. Electronic equipment on board all spacecrafts is exposed to this radiation which can reduce the lifetime of a craft and even cause mission failure. An understanding of radiation and the development of radiation tolerant electronic design techniques is required for the safe and successful exploration of space. The technique of designing and fabricating electronic systems to withstand radiation is called *radiation hardening*.

Phase-locked loops (PLLs) are an integral part of many electronic systems. They are used for a number of applications like clock synthesis in microprocessors, synchronizing data transmission, local frequency synthesis in wireless transmission, etc. Radiation hardening of phase-locked loops is essential for all these applications. This report summarizes the effects of radiation on phase-locked loops and describes a scheme to design radiation hardened phase-locked loops.

The effects of radiation are both instantaneous and long-term. The instantaneous effects of the collision of a high-energy particle with an active device are

called *single-event effects* (SEE). The cumulative effects of several such collisions over a long period of time are called *total ionization dose* (TID) effects. The objective of this project is to develop phase-locked loops that are tolerant to both these effects.

1.2. Organization

Chapter 2 begins with the description of the effects of radiation on active devices (MOSFETs in particular). This is followed by a description of the effects of TID and SEE on various building blocks of a PLL. Chapter 3 describes the architecture of a digital phase locked loop (DPLL) and its various basic building blocks. A linearized analysis of the digital PLL is also presented here. Chapter 3 also describes various radiation hardening techniques that can be employed to withstand the effects of total dose and single event effects. The summary of this work and conclusions follow in Chapter 4.

2. EFFECTS OF RADIATION ON PHASE-LOCKED LOOPS

2.1. Effect of total ionization dosage on transistors

Total ionization dose (TID) effects on active devices are a consequence of long-term exposure of electronic components to radiation. The amount of ionization dose depends on the intensity of radiation and the period of exposure [1]. This effect primarily results in shift of transistor threshold voltage values as a function of dose [2]. Additionally, TID also results in gate oxide leakage.

2.1.1. Threshold voltage shift

Threshold voltage shift is a consequence of accumulation of charge in the gate oxide in MOS transistors. Fig. 2.1 illustrates the mechanism by which charge is accumulated at the Si-SiO_2 interface in a transistor. As a high energy particle tunnels through the active device, it ionizes the material in its wake. This is a result of transfer of energy from the high-energy particle to the material. To create an electron-hole (e^--h^+) pair in Si, the energy required is 1.1eV. Similarly, it takes

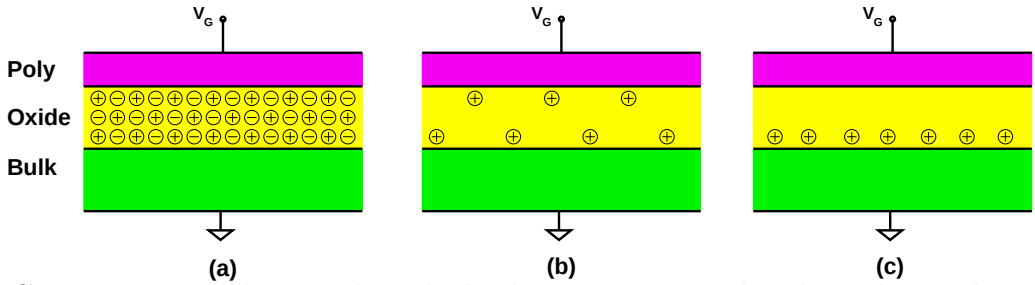


FIGURE 2.1. Mechanism by which charge is accumulated in the oxide. (a) Ionization following a heavy ion strike, (b) Electrons drift and holes remain, (c) Holes drift towards the Si-SiO_2 interface.

17eV to create a e^--h^+ pair in SiO_2. The particle creates several such e^--h^+ pairs in the oxide and bulk. The electrons generated in the oxide are relatively mobile and drift out of the oxide [2]. However, the holes are heavier and less mobile. The time-constants of electron and hole mobilities in the oxide are in the order of pico-seconds and milli-seconds respectively. The holes drift towards the Si-SiO_2 interface in a NMOS transistor and accumulate at the surface. This accumulation of positive charges in the oxide reduces the threshold voltage of an NMOS device.

$$V_{th}^{rad} = V_{th}^{0} - \frac{Q_{ox}}{C_{ox}} \tag{2.1}$$

where, V_{th}^{0} is the nominal threshold voltage; V_{th}^{rad} is the threshold voltage after radiation; Q_{ox} is the charge-density in the oxide and C_{ox} is the oxide (SiO_2) capacitance per unit area. This accumulation of holes inside the oxide tends to reduce the threshold voltage of NMOS transistors and increases the threshold voltage of PMOS transistors. This effect is critical in advanced processes with low supply voltages. Exposure of a circuit to large doses of radiation can prevent the NMOS devices from switching off and the PMOS devices from switching on.

2.1.2. Gate leakage current

The gate current leakage in MOS transistors is enhanced as a result of radiation. Gate leakage occurs as a result of tunneling of electrons through the thin gate oxide layer. This is compounded by the scaling of device feature sizes. The trapped charges in the oxide act as an intermediate state in the transfer of electrons through the oxide [1]. This trap assisted tunneling is attributed as the reason for enhanced gate current leakage. Fig. 2.2 shows the enhancement of gate current leakage as a result of TID.

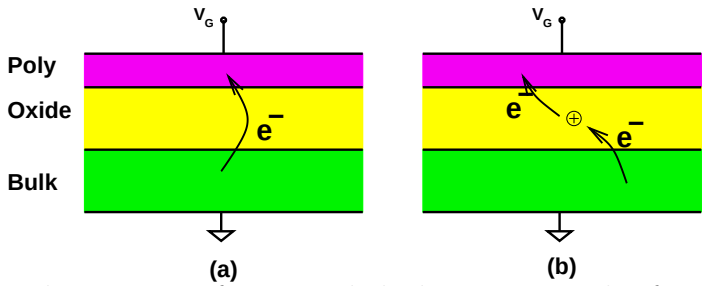


FIGURE 2.2. Enhancement of gate oxide leakage as a result of TID. (a) Electron tunneling through the oxide. (b) Trap assisted tunneling through the oxide.

2.1.3. Shielding

In order to reduce the extent of exposure of a circuit to radiation, it is shielded by several layers of metal. The payload considerations of a spacecraft limit the thickness of the shielding metal. The metal layers are at best able to stop the low energy particles. The high energy particles are able to penetrate the metal shielding. It is also reported that increasing the thickness of the shielding results in diminishing returns beyond a particular thickness [1].

2.1.4. Effect of device scaling

The charged particle concentration generated is proportional to the volume of the gate oxide. Reducing gate oxide thickness reduces the accumulated charge. Hence, processes with thinner gate oxides are best suited for radiation hardened applications. As the device dimensions are reduced, the gate oxide thickness is also reduced. Hence, advanced processes exhibit a smaller shift in threshold voltages.

2.1.5. Annealing

Annealing of a radiated device can counter the effects of radiation. This occurs as a result of electron tunneling through the Si-SiO_2 interface. When the electrons in the channel are excited thermally or through high electric fields, they cross the Si-SiO_2 interface energy barrier. These electrons can recombine with the trapped positive charges in the oxide. This tends to offset the effects of TID [1]. However, the rate of annealing is slower than the trapped charge generation.

In summary, the total dose causes the threshold voltages of active devices to shift and enhances the gate leakage current. The reduction in threshold voltage of NMOS transistors can prevent them from switching off. This would result in power dissipation in the device due to subthreshold operation even in the off-state. The V_{th} increase in PMOS transistors can prevent them from switching on. This shift in threshold voltages can eventually cause functional failure of a circuit. The threshold voltage shift becomes more significant with device and voltage scaling. Digital circuits employ transistors as simple switches. Hence, digital blocks are inherently tolerant upto moderate doses of radiation. However, analog designs are more involved and these blocks suffer more severely due to shifts in threshold voltages. In general, TID increases the speed of NMOS transistors and slows down PMOS transistors for the same V_{gs}.

2.2. Single Event Effects

Single event effects are the events that occur as a result of a high energy particle striking a semiconductor device [1]. As the particle transverses through the device, it transfers energy to the material. Linear energy transfer (LET) is the term used to describe the capacity of a particle to deliver energy to the device.

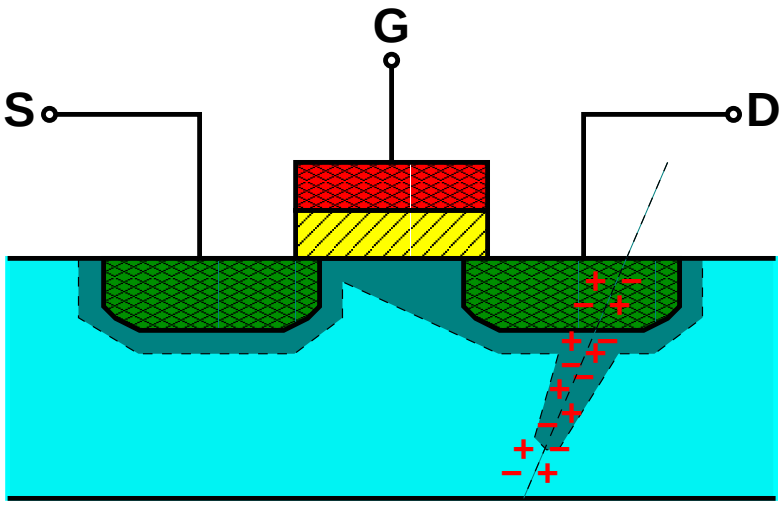


FIGURE 2.3. Ionization track in a NMOS transistor in the wake of a high energy particle strike.

It is the amount of energy deposited per unit distance traveled, normalized to the material's density [3]. This is expressed as MeV-cm^2/mg. This energy is responsible for ionization of the material in the wake of the particle's trajectory through the semiconductor. Fig. 2.3 shows the ionization track in the wake of a high energy particle in a NMOS transistor. Through the principle of conservation of energy, the loss of kinetic energy of the particle is proportional to the ionization energy delivered to the material. The amount of charge generated as a result of the strike can be calculated as the energy delivered divided by the energy required to generate one electron-hole pair in silicon. The amount of charge generated in the semiconductor as a result of ionization is proportional to the LET of the particle.

2.2.1. SPICE model

The charge generated in the semiconductor device drifts as a result of the electric fields. This charge drift results in a transient current for a short duration in

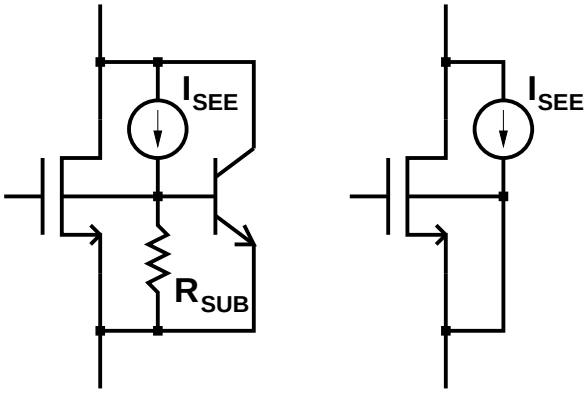


FIGURE 2.4. Transistor models for SEE. (a) SOI NMOS model. (b) Simplified model.

the device. This current is usually modeled as a sum of three exponential current sources [4, 5]. Two current sources are used to model the exponentially decaying hole and electron drift current components. A third source models the slowly varying current as a result of diffusion of the generated carriers. The electron and hole currents exhibit different time-constants as a result of the difference in mobilities. The suggested SPICE model [4, 5] to be used for simulations can be seen in Fig. 2.4.

2.2.2. Single Event Latchup

Single event latchup (SEL) occurs when current flows unregulated through the parasitic thyristor structure in CMOS technology [3]. When the current through the thyristor structure exceeds a threshold current, this structure latches up and allows a constant current to pass through it. Fig. 2.5 shows the parasitic thyristor structure in a bulk CMOS technology. A high energy particle strike can cause such an event to occur. This happens because of the regenerative feedback

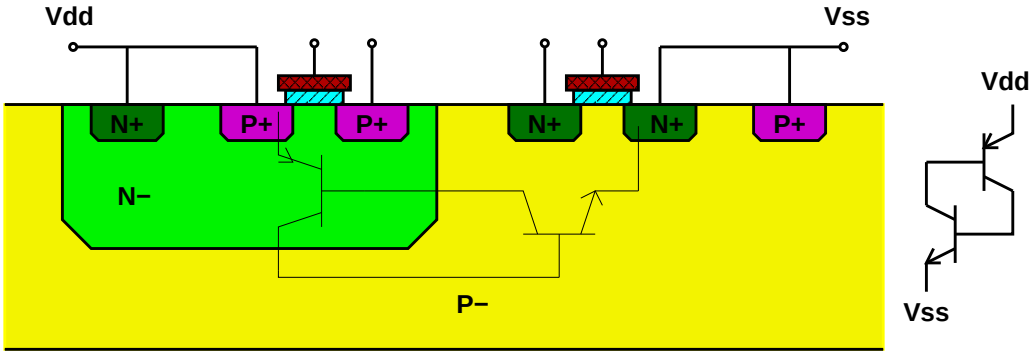


FIGURE 2.5. Single event latchup phenomenon in bulk CMOS technology.

in the n-p-n and p-n-p structure. As a result, there is a constant current flow from the supply to ground. This could cause the device to heat up and eventually burn out. The circuit can be restored to normalcy only by powering down the circuit. In order to avoid this, conventional CMOS circuits implement automatic power down on detection of high currents through the supply. Some systems also implement periodic shutdown of circuit blocks. SOI CMOS has its NMOS and PMOS transistors in individual islands. There is no parasitic thyristor in this technology, and as a result SOI CMOS is latchup free.

2.2.3. Dependence on process technology

The amount of charge accumulated is proportional to the volume of the active device. This volume is significantly lower in SOI CMOS devices compared to a conventional bulk CMOS technology. The amount of charge collected as a result of a strike is significantly lower. This is another strong incentive for using SOI CMOS in radiation hardened applications. The probability of a heavy ion striking a device is proportional to its area. Hence, a larger device is more likely to be hit than a smaller device. On the other hand, a larger device has

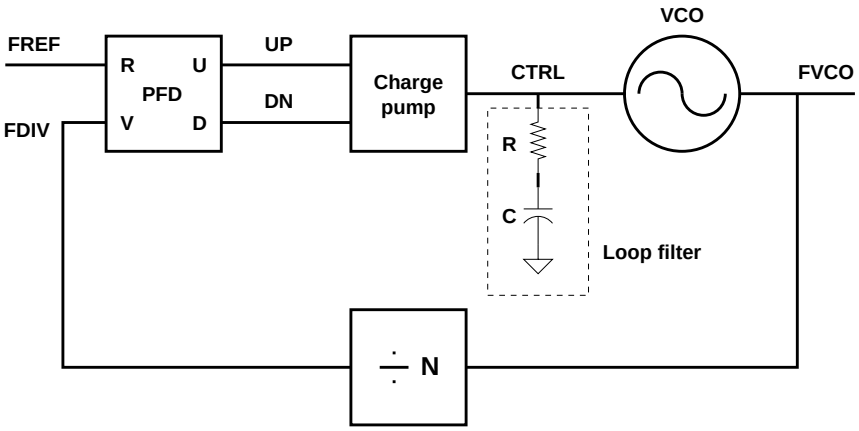


FIGURE 2.6. A generic phase-locked loop

more capacitance than a smaller device and the resulting voltage transient in a larger device is smaller. Digital circuits are less sensitive to voltage transients during static phases. They require error voltages about half the supply voltage to cause an error. However, structures with regenerative feedback (memories) during switching can latch to incorrect values as a result of a heavy ion strike. A heavy ion strike resulting in a latch recording an incorrect digital value is called a *single event upset* (SEU). In conclusion, SOI CMOS technology is favored in radiation hardened applications. SEE becomes more significant with device scaling.

2.3. Operation of Phase-Locked Loop

Phase-locked loops are employed to generate high-frequency clock signals and local carriers in wireless systems. Fig. 2.6 shows a typical phase-locked loop. The building blocks of a phase-locked loop are (a) voltage controlled oscillator (VCO), (b) frequency divider, (c) phase/frequency detector (PFD) (d) charge pump, and (e) loop filter.

The PLL operates as follows. The PFD generates UP and DN pulses which give the phase difference between the reference (FREF) and the divided (FDIV) clocks. This phase difference is converted to a current through the charge pump. The loop filter filters this current to generate the required control voltage that controls the frequency of operation of the VCO. The negative feedback around the PLL ensures that the reference and divided clocks are in phase lock. The VCO output frequency to the reference frequency is maintained at a constant ratio fixed by the frequency division ratio.

2.4. Effects of TID in PLLs

Test oscillators and phase-locked loops were designed and fabricated in the Honeywell 0.35μm SOI CMOS process. These test oscillators and PLLs were characterized and were then exposed to radiation. The characteristics were recorded as a function of radiation dosage. The design of these test blocks and the measurement results are reported in [6–9].

The test results indicate that the VCO tuning characteristics and charge pump bias currents change as a result of total dose. As a result the loop characteristics such as loop gain, bandwidth and damping also change. This could result in peaking in the jitter transfer function and deterioration in performance.

2.5. Single Event Effects in PLL

2.5.1. Voltage Controlled Oscillator

SEE can occur on any of the output nodes of a ring oscillator and cause the output to deviate from its projected trajectory. This can be modeled as a

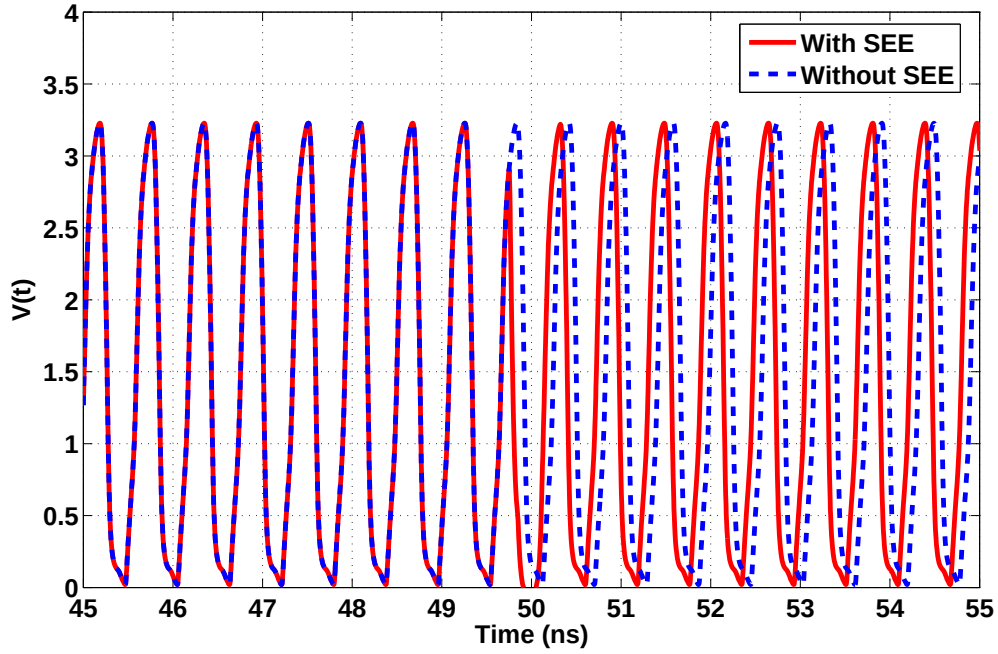


FIGURE 2.7. SEE on one of the delay cells of a Lee/Kim ring oscillator.

phase disturbance at the output of the oscillator. Fig. 2.7 shows the effect of SEE on a Lee/Kim ring oscillator [10]. The dotted line indicates the output of a normal oscillator. The solid line indicates the output of the oscillator when it is hit. It can be observed that SEE causes a small timeshift in the operation of the oscillator.

When such a ring oscillator is employed in a PLL, the loop would eventually correct the output. It should also be noted that the penalty of such a hit is less serious.

2.5.2. Frequency Divider

Frequency dividers are usually implemented as a cascade of divide-by-two stages. Each of these stages is a D-flipflop in feedback. The output of the divide-by-two stage toggles every rising edge of the input. A particle strike on any of the divider stages can cause it to miss a transition. Therefore, SEE on the first few stages of the frequency divider causes a small jitter in the output of the PLL. However, a hit on the last few stages of the frequency divider can be serious. This could cause the PLL to go out of lock and the PLL requires several time-constants to restore normalcy. Fig. 2.8 shows the effect of SEE on the last stage of a frequency divider. As a result of the hit, the PLL loses lock and is restored after several micro-seconds. Hence, a hit on any of the last few stages of the divider could be disastrous depending on the application.

2.5.3. SEE on Phase/Frequency Detector

A hit on the phase detector would be similar. This would cause a huge error at the input of the PLL making the PLL lose lock. Several time constants will be required to restore lock.

2.5.4. SEE on Charge Pump and Loop Filter

The output node of the charge pump is the most sensitive node in a PLL. A hit on any of the transistors connected to the loop filter would cause a transient error current at this node. This current would upset the control voltage of the PLL. This would cause the PLL to lose lock. Fig. 2.9 shows the effect of SEE on

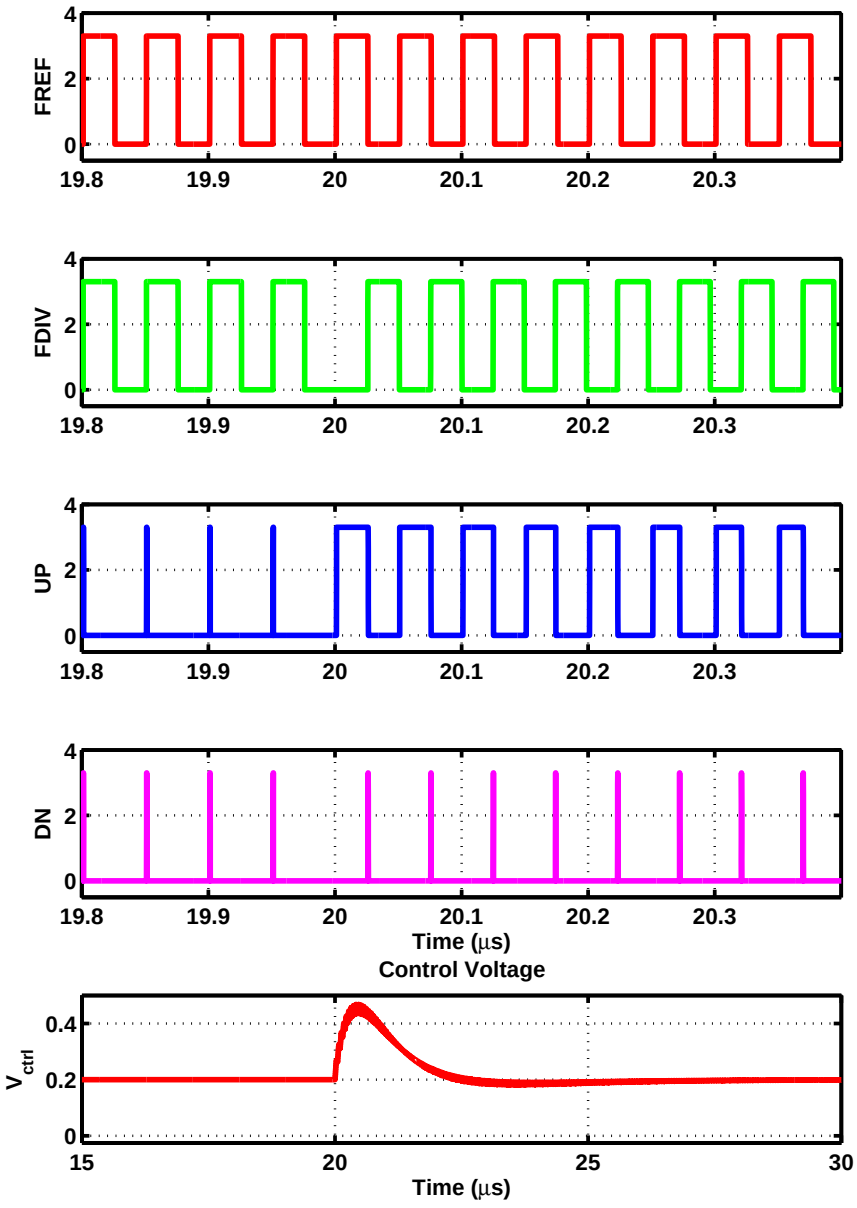


FIGURE 2.8. SEE on the last stage of the divider chain.

the charge pump output node. It can be seen that the error transient causes the PLL to go out of lock and the lock is restored after several micro-seconds.

A large capacitor on the loop filter would be able to absorb large amounts of currents producing smaller amounts of voltage change. However, a larger capacitor would imply a smaller bandwidth and a slower lock restoration process.

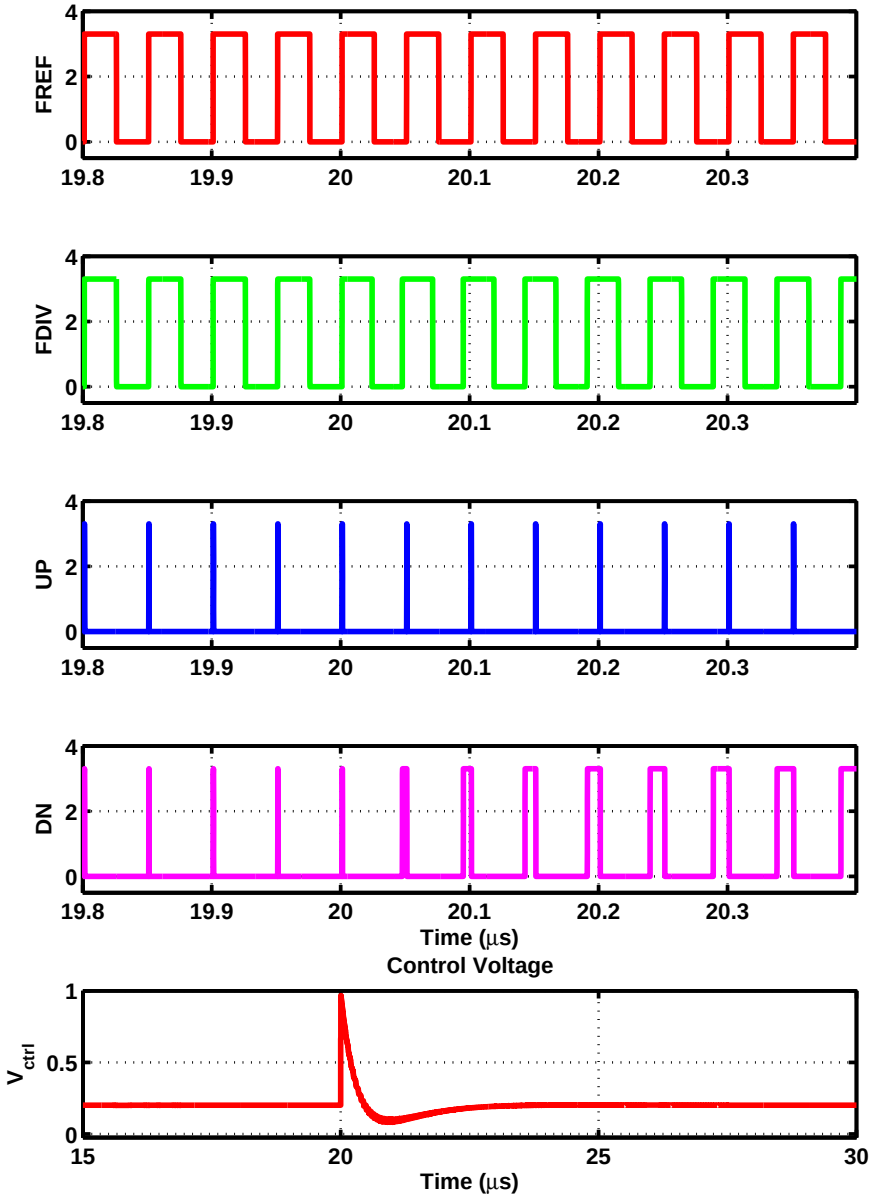


FIGURE 2.9. SEE on the transistor connected to the output node of a charge pump.

3. DESIGN OF A DIGITAL PHASE LOCKED LOOP

Total ionization dose causes the PLL loop parameters to change. This could cause peaking in the jitter transfer function and deterioration in its performance. Single event strike on frequency divider, phase detector or loop filter can cause the PLL to lose phase lock. The phase lock is eventually restored after several micro seconds. Digital blocks are less sensitive to variations in transistor threshold voltages. Digital systems are also amenable to implementation of redundancy and error correction techniques. Hence, a digitally intensive PLL with error correction techniques is ideal for radiation hardened applications. Such digital PLLs can also incorporate startup calibration techniques to compensate for variations in loop parameters [11, 12].

The digital phase-locked loop (DPLL) designed and implemented is similar to [12]. The architecture of the DPLL can be seen in Fig. 3.1. The basic building blocks of a DPLL are (a) digitally controlled analog oscillator (DCAO), (b) frequency divider, (c) phase/frequency detector (PFD), (d) time-to-digital converter (TDC) and (e) digital controller / loop filter (LF). The design and implementation of each of the building blocks is explained in the following section.

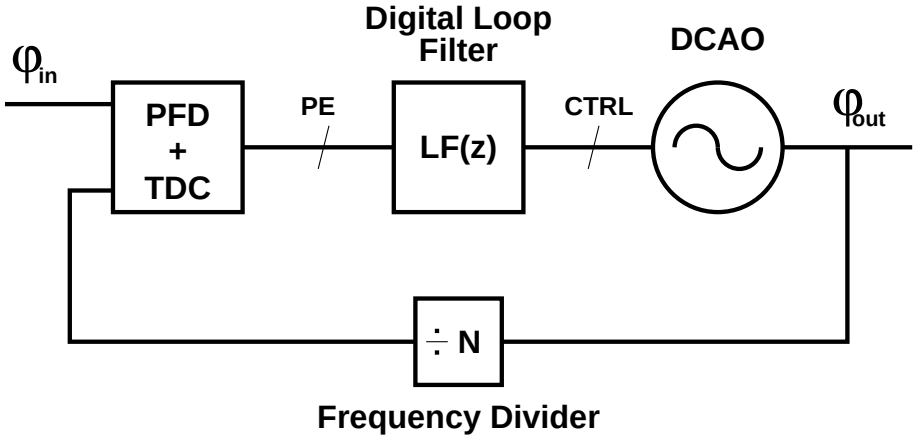


FIGURE 3.1. Architecture of a digital PLL.

3.1. Building Blocks of a Digital PLL

3.1.1. Digitally controlled analog oscillator (DCAO)

The DCAO is implemented as a three stage differential ring oscillator. The differential delay cell is a Lee/Kim delay cell with coarse and fine controls. Fig. 3.2 shows the schematic of the differential delay cell. The tail current through the delay cell is controlled by a bank of current sources. The tuning word is comprised of coarse and fine bits. The coarse and fine tuning bits are converted to a current using a binary weighted current DAC. The schematic of the fine tuning bit current DAC can be seen in Fig. 3.3. The coarse bits employ a similar DAC to generate a coarse tuning voltage. In the current DAC, the tuning bits DF[0-N] switch the current being drawn through PM1. The current through PM1 in turn generates a fine tuning control voltage. In the current design there are six fine tuning bits and six coarse tuning bits. This makes up for a total of twelve tuning bits. The tuning voltages 'Vcoarse' and 'Vfine' that are generated are used to control the current through the delay cell. The resistor 'Rfine' allows for the control of a unit current mirrored through the circuit. This can be adjusted through an off-chip potentiometer to control the current. The tuning bits provide a digital control of the oscillation frequency of the oscillator.

3.1.2. Frequency divider

The frequency divider is implemented as a cascade of divide-by-two stages. Each stage is a true single phase clock (TSPC) logic flip-flop [5] in feedback. A circuit diagram of the flip-flop and a single divide-by-two stage is shown in Fig. 3.4. The output of the displayed stage toggles at every rising edge of the clock.

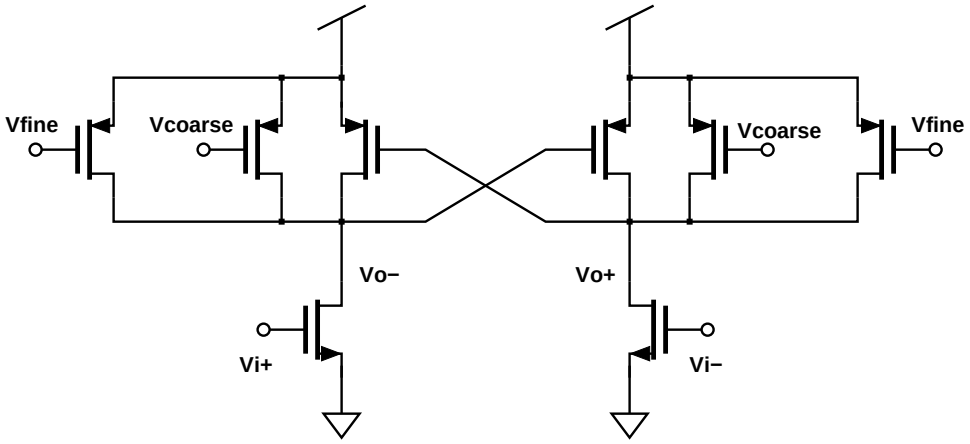


FIGURE 3.2. Lee/Kim differential delay cell with dual tuning inputs.

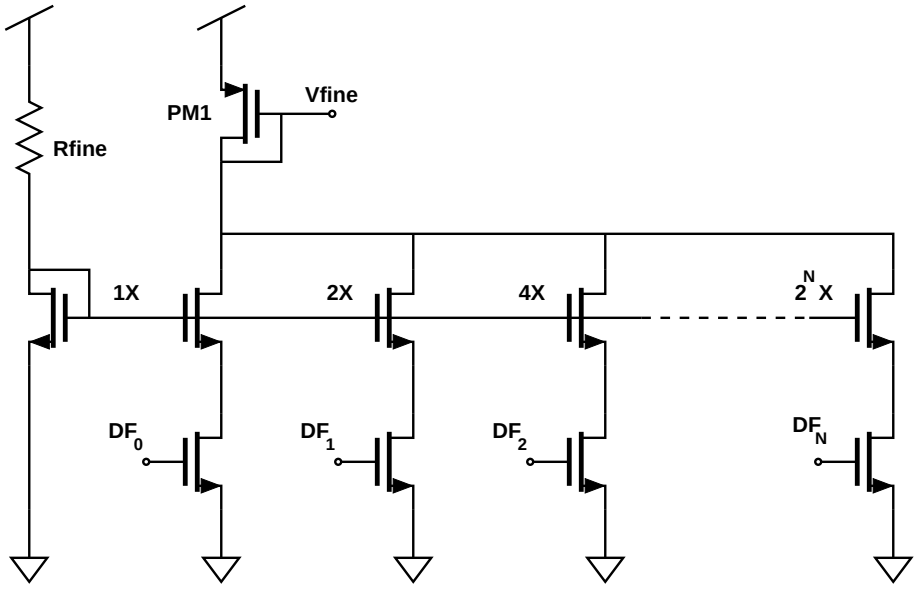


FIGURE 3.3. Fine tuning control circuit.

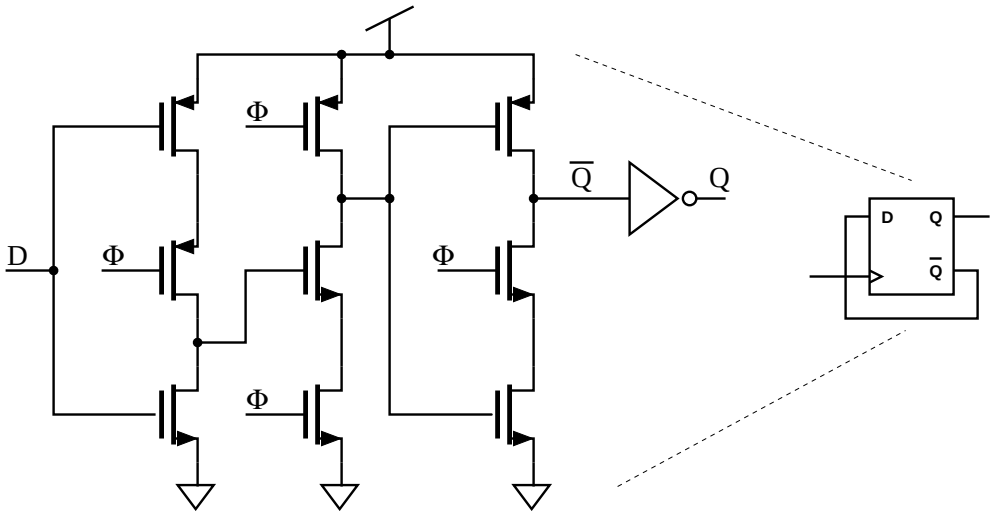


FIGURE 3.4. TSPC flip-flop and a divide-by-two stage.

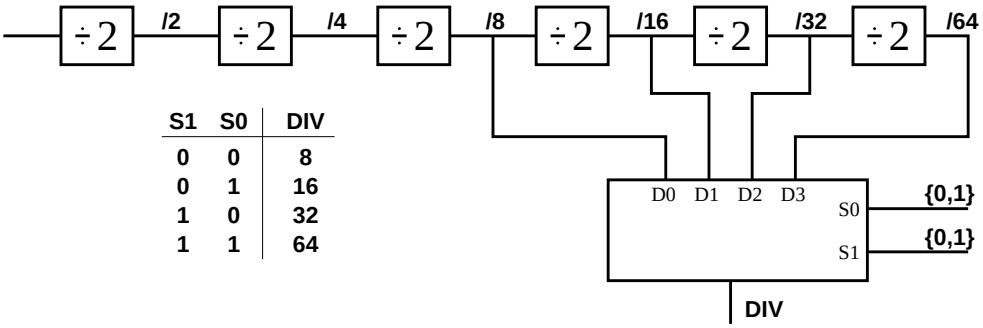


FIGURE 3.5. Programmable frequency divider.

Hence, the output frequency is half that of the input frequency. Higher frequency division ratios can be achieved by cascading such stages. In order to make the division ratio programmable a multiplexer has been added to enable us to select from a choice of division ratios. The schematic diagram of the programmable frequency divider is shown in Fig. 3.5. The possible division ratios are 8, 16, 32 and 64. They can be selected using the control bits S1 and S0.

3.1.3. Time-to-digital converter

The time-to-digital converter compares the input reference clock and the oscillator divided output and generates the phase difference word. Fig. 3.6 shows the schematic of the time-to-digital converter and Fig. 3.7 shows the operation of the time-to-digital converter.

The TDC operates as follows. The phase/frequency detector (PFD) at the input of the TDC generates UP and DN pulses. A digital OR gate generates the $UP + DN$ pulse whose width is equal to the width of the wider of the two pulses. The delay chain in a TDC generates delayed versions (D1, D2, ..., D8) of the $UP + DN$ pulse. When these delayed versions are latched by the rising edge of the $\overline{UP + DN}$ pulse, the number of latch outputs that are high is the width of the $UP + DN$ pulse expressed as a number of inverter delays. The sign of the phase error is evaluated by latching the DN pulse using the UP pulse. The sign would be high when the DN pulse precedes the UP pulse, i.e., the phase error is negative. A matching delay circuit is implemented using current starved inverters to compensate for the finite width of the UP/DN pulses in an actual PFD. A linear delay chain would require a large number of inverters and latches to cover the entire range. An exponential delay chain covers a wider range with fewer stages. The initial stages of the exponential delay chain have minimum possible delays to provide finer resolution and the subsequent stages have larger delays to cover a wider range. The minimum delay is the resolution of the TDC. It is denoted by dT and is about 80-100ps in the given process. This delay includes the effects of the loading of the subsequent stages and the latch. The value of the delay elements in the delay chain are dT, dT, dT, 4dT, 8dT, 16dT, 32dT, 64dT and 128dT. These nine stages cover a delay range of dT-256dT. The possible output

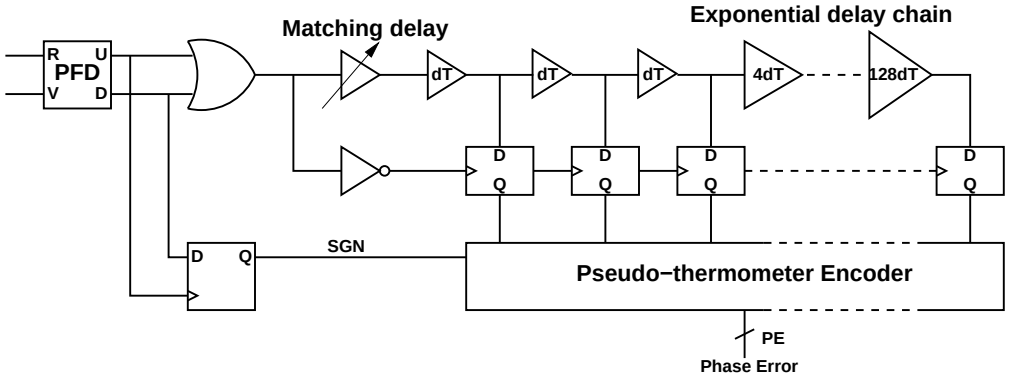


FIGURE 3.6. Time-to-digital converter.

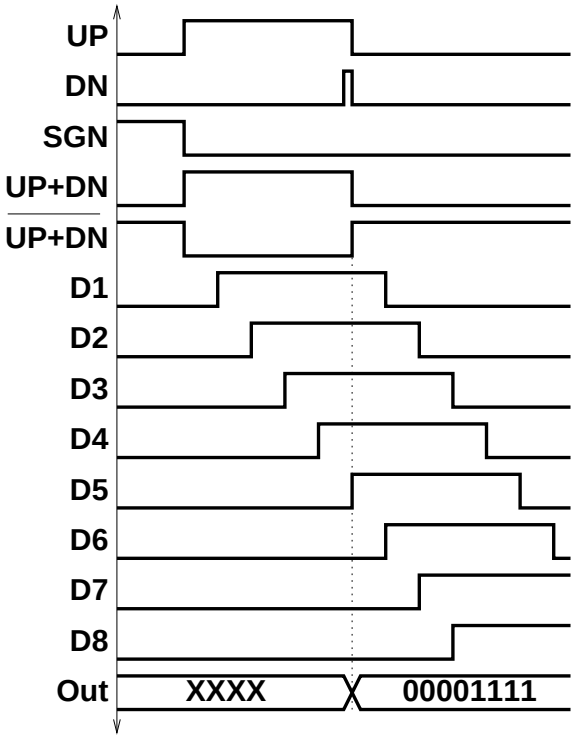


FIGURE 3.7. Operation of a time-to-digital converter.

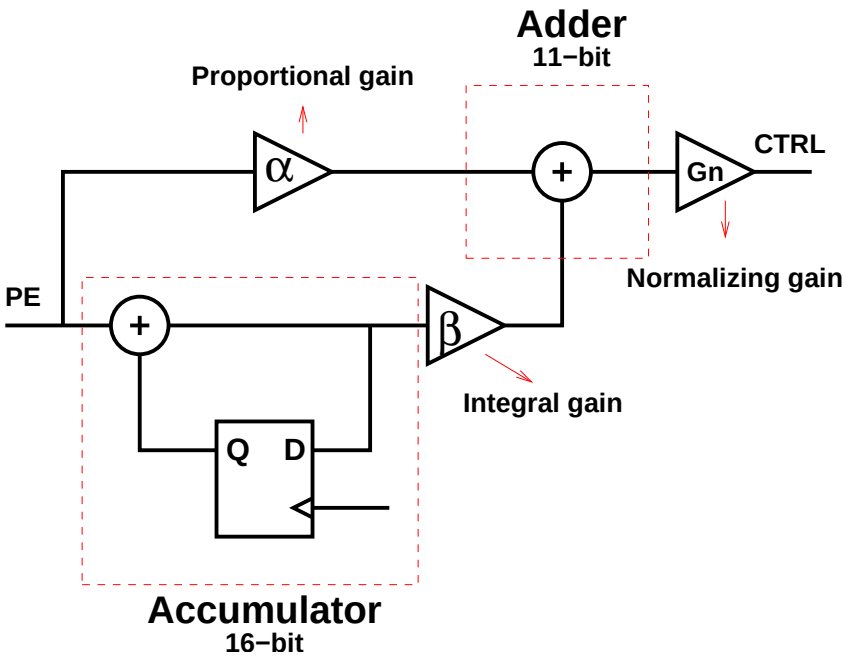


FIGURE 3.8. Proportional-integral controller loop filter.

values of the TDC are -256 to 256 in conjunction with the sign bit. The latch outputs are converted to a 10-bit 2's complement signed digital word through the pseudo-thermometer encoder. Due to the exponential nature of the delay chain, the design of the encoder is greatly simplified.

The resolution of this TDC is limited by the inherent delay of a digital inverter. A statistical TDC that overcomes the resolution limitation imposed by gate delays by relying on the statistical variation of offsets was proposed in [13]. This TDC would greatly enhance the performance of the digital PLL. Such a TDC prototype was implemented along side the digital PLL [14].

3.1.4. Digital proportional-integral controller

The loop filter in the digital PLL is a proportional-integral (PI) controller

with a proportional and an integral path. The former is analogous to the resistor in a charge pump PLL, while the latter is comparable to the capacitor. Fig. 3.8 shows the architecture of the loop filter. The integral path consists of an accumulator and a gain β. The proportional path has a gain α. The outputs of the proportional path and the integral path are added and normalized to give the control word. The length of the accumulator register is 16-bits. This accumulator is implemented by stacking 16 single-bit accumulators. A schematic showing the single-bit accumulator and the 16-bit accumulator is shown in Fig. 3.9. The latch used in the accumulator is shown in Fig. 3.10 and the mirror adder circuit has been shown in Fig. 3.11. Implementing the proportional and integral gains requires digital multipliers. However, multiplication by powers of two can be achieved by adding zeros at the end of a word or truncating bits. The proportional gain is set to one and the integral gain was set to 2^{-5}. To keep the jitter arising from the discrete nature of digital PLL low, the normalizing gain has to be less than 1 and has been set to 0.5. Fig. 3.12 shows the implementation of these gains in the digital PLL.

The accumulator and the adder in the loop filter can overflow and give erroneous outputs. This can be prevented by implementing saturating adders. An overflow occurs when the inputs are positive and the output is negative. Similarly, an underflow occurs when the inputs are negative and the output is positive. An error cannot occur when the inputs have opposite signs. The saturating adder detects an overflow or an underflow and limits it to the highest (2N-1) or lowest (-2N) values. The schematic of the implemented saturating adder is shown in Fig. 3.13.

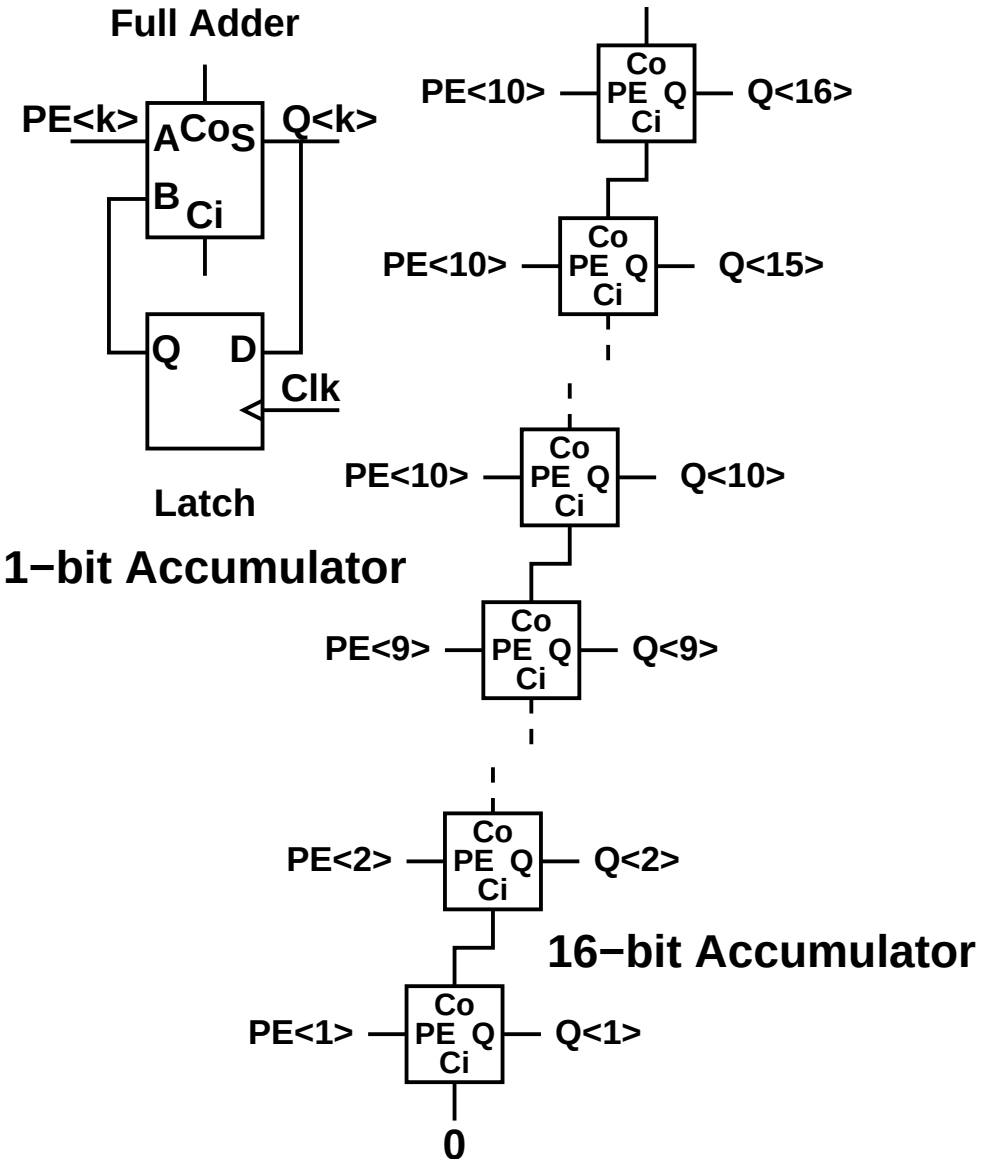


FIGURE 3.9. 1-bit accumulator and 16-bit accumulator.

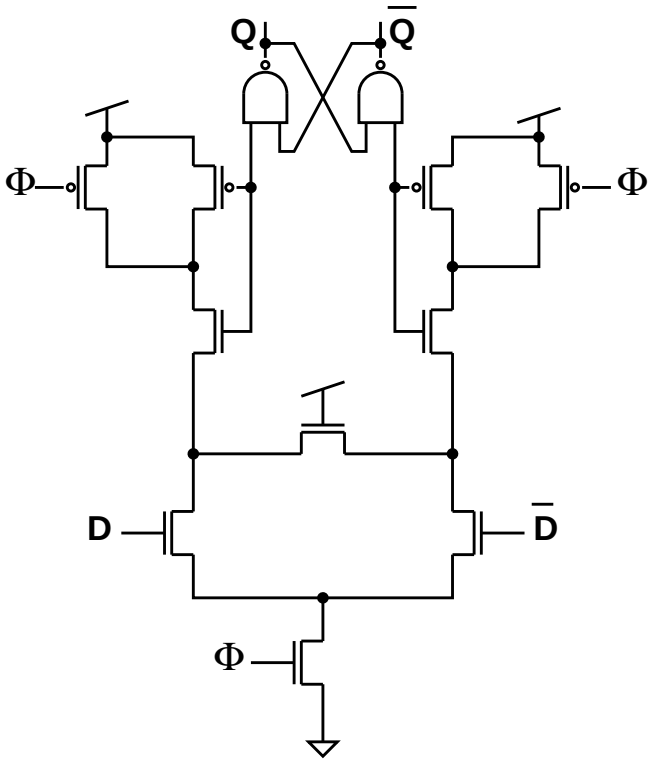


FIGURE 3.10. Sense-amplifier flip flop.

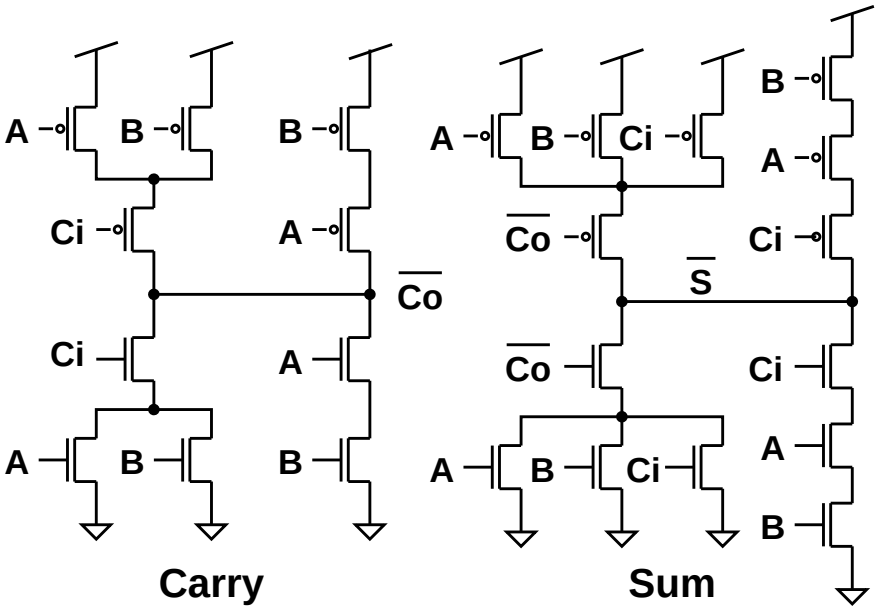


FIGURE 3.11. CMOS mirror adder circuit.

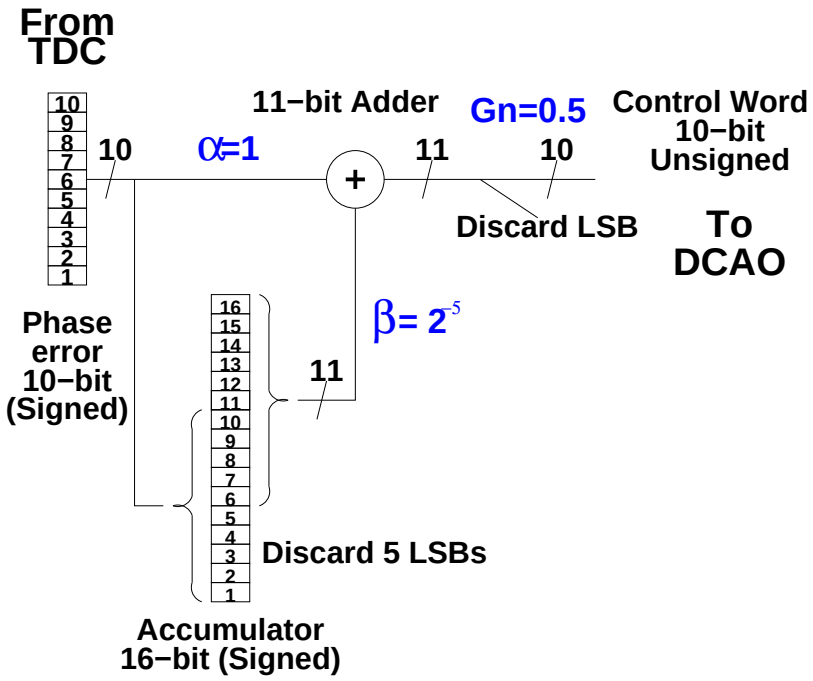


FIGURE 3.12. Digital PLL controller.

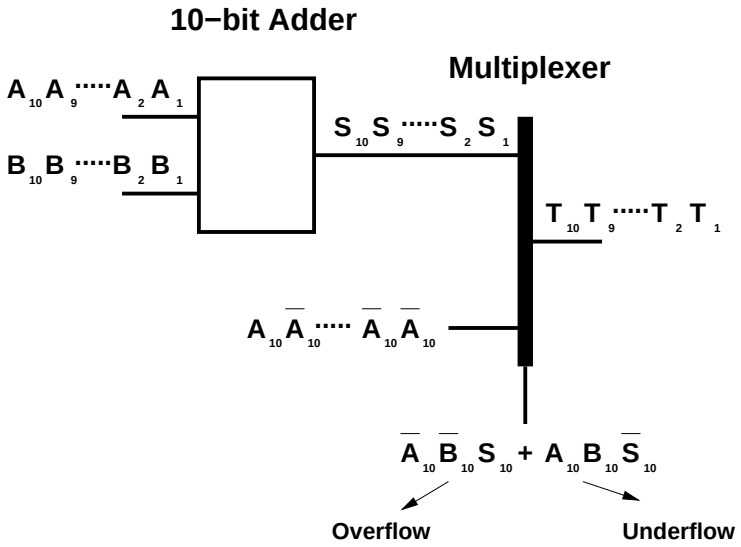


FIGURE 3.13. Saturating adder.

3.2. Analysis of Digital Phase Locked Loops

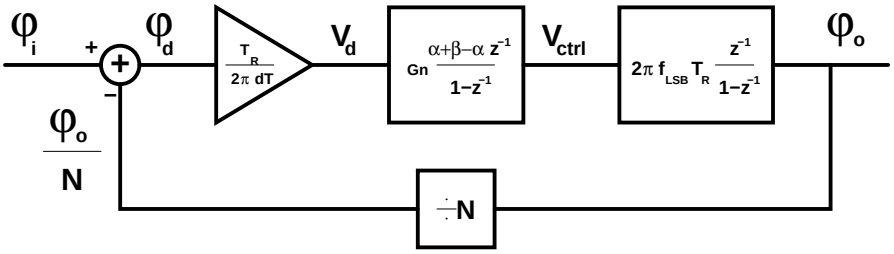


FIGURE 3.14. z-domain model of the digital PLL.

The z-domain model of the digital PLL is shown in Fig. 3.14. Let $\phi_i[n]$ and $\phi_o[n]$ be the input and output sampled at every reference cycle. The phase accumulated by the output of the DCAO every reference cycle is proportional to the control word $v_{ctrl}[n]$:

$$\phi_o[n+1] - \phi_o[n] = 2\pi f_{LSB} T_R v_{ctrl}[n] \tag{3.1}$$

$$\frac{\phi_o(z)}{V_{ctrl}(z)} = 2\pi f_{LSB} T_R \frac{z^{-1}}{1-z^{-1}} \tag{3.2}$$

where, f_{LSB} is the resolution of the DCAO and T_R is the period of one reference cycle.

For a phase error of 2π, the output of the TDC is T_R/dT. Here, dT is the resolution of the TDC.

$$v_d[n] = \frac{1}{2\pi}\frac{T_R}{dT}\phi_d[n] \tag{3.3}$$

The output of the loop filter is the scaled sum of the proportional and integral paths.

$$V_{ctrl}(z) = G_n\left(\alpha + \frac{\beta}{1-z^{-1}}\right) V_d(z) \tag{3.4}$$

$$\frac{V_{ctrl}(z)}{V_d(z)} = G_n \left(\frac{\alpha + \beta - \alpha z^{-1}}{1 - z^{-1}} \right) \tag{3.5}$$

The loop gain of the digital PLL is given by

$$\frac{\phi_o(z)}{\phi_i(z)} = \frac{1}{N} G_n \frac{T_R}{dT} f_{LSB} T_R \left(\frac{\left(\alpha + \beta - \alpha z^{-1}\right) z^{-1}}{1 - z^{-1}} \right) \tag{3.6}$$

and the closed loop gain is

$$\frac{\phi_o(z)}{\phi_i(z)} = \frac{K_{dig} \left(\alpha + \beta - \alpha z^{-1}\right) z^{-1}}{1 - \left(2 - \frac{K_{dig}}{N}(\alpha + \beta)\right) z^{-1} + \left(1 - \frac{K_{dig}}{N}\alpha\right) z^{-2}} \tag{3.7}$$

where, $K_{dig} = G_n(T_R/dT) f_{LSB} T_R$.

3.3. Analogy to an Analog PLL

Digital systems are difficult to understand and conventional analog methods are often used to study and understand the digital systems. The concepts of loop gain, phase margin, bandwidth, damping, etc., are easy to understand and analyze in continuous-time systems. Hence, an analogy with the charge pump PLL (CPPLL) is presented here. For a CPPLL with loop gain K_{CP}, and a zero at ω_z, the loop gain is expressed as:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{1}{N} \frac{K_{CP}}{s^2} (s + \omega_z) \tag{3.8}$$

The digital PLL implemented can be correlated with a CPPLL using the bilinear transform. This transform is used to obtain the equivalent z-domain transfer function from a s-domain transfer function. In this transform, the 's' term is replaced by $\frac{2}{T_s}\frac{z-1}{z+1}$. Using this transform, the s-domain and z-domain models are connected by the following equations.

$$\frac{\beta}{\alpha} = \frac{\omega_z}{F_R} \tag{3.9}$$

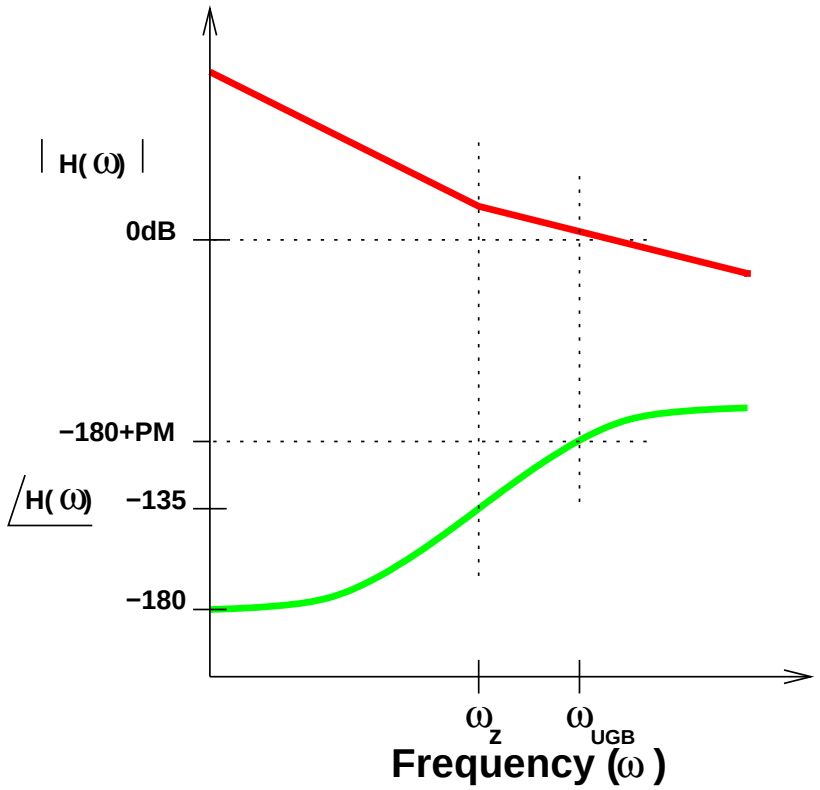


FIGURE 3.15. Magnitude and phase response of a 2nd-order PLL.

$$K_{CP} = K_{dig} F_R \tag{3.10}$$

where, F_R is the update frequency of the digital PLL ($T_R = 1/F_R$). This correlation can be used to design digital PLLs with a specified phase-margin and bandwidth.

A method to evaluate the loop parameters for a given DCAO and TDC resolution and phase margin is described below. Fig. 3.15 shows the magnitude and phase response of a 2^{nd} order PLL. In a 2^{nd} order system, the phase margin is the contribution of the zero at the unity gain frequency.

$$\Phi_M = tan^{-1}\left(\frac{\omega_{UGB}}{\omega_z}\right) \tag{3.11}$$

And the unity gain frequency is given by

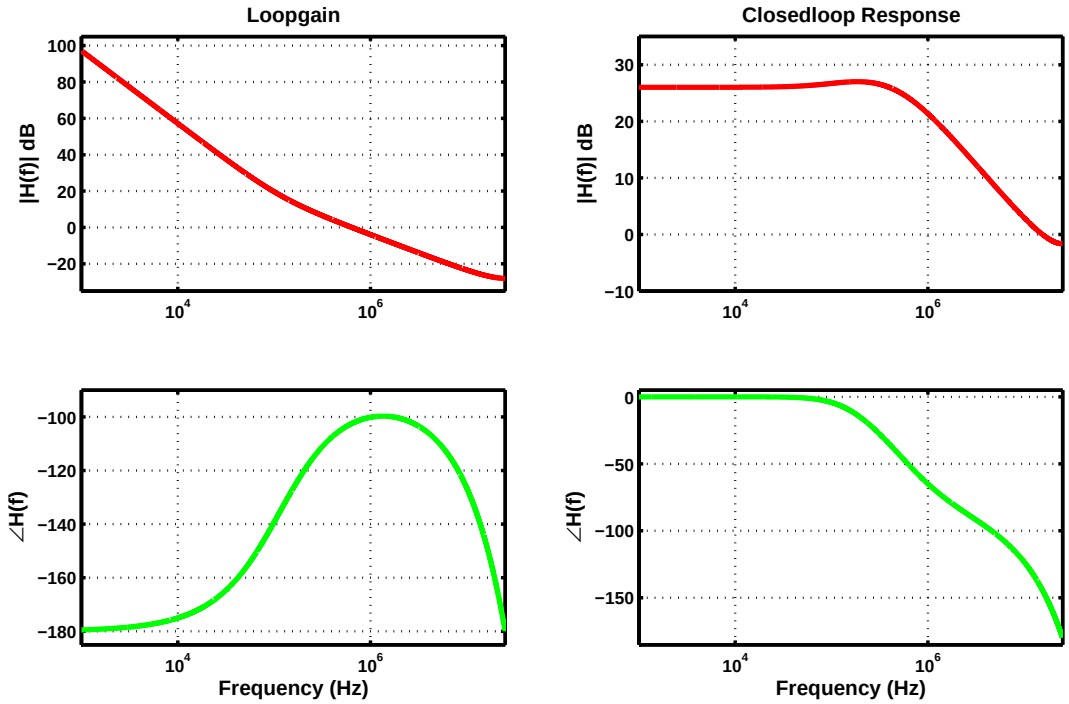


FIGURE 3.16. Frequency response of the digital PLL estimated from the loop parameters.

$$\omega_{UGB} = \frac{K_{dig} F_R}{N} \sqrt{1 + tan^2\left(\Phi_M\right)} \tag{3.12}$$

The above equations give the unity gain frequency and the maximum value of the zero frequency that gives the required phase margin. These equations can be used to estimate the required value of β.

For a digital PLL with f_{LSB}=200kHz, dT=50ps, N=20, F_R=50MHz (F_{vco}=1GHz), Φ_M=80^o, G_n=0.5 and α=1, the estimated value of β = 0.01432 and $f_{UGB} = 646kHz$. Simulink models for this digital PLL were simulated and the transient performance of the model agrees with the z-domain model. Fig. 3.16 shows the response of the digital PLL plotted using MATLAB. This figure shows

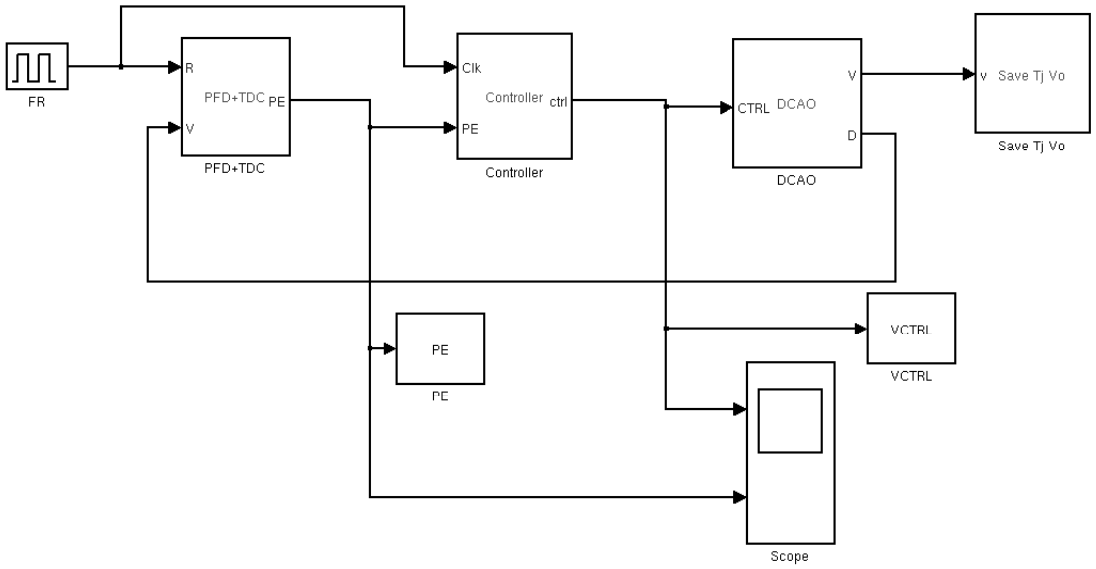


FIGURE 3.17. Simulink model used to verify the operation of a digital PLL.

that the CPPLL analogy can be employed to estimate the coefficients of a digital PLL.

3.4. Behavioral Model

A Simulink model of the digital PLL was constructed to simulate its operation. A schematic of this model is shown in Fig. 3.17. This model uses many of the standard blocks provided in Simulink to build the various building blocks of a digital PLL.

The Simulink model provides valuable insight into the operation of a digital PLL. This also helps in making design choices over various kinds of implementations. Fig. 3.18 shows the response of the Simulink model to a frequency step at the input of the digital PLL. The figure shows good agreement with the analytical model described in Section 3.2.

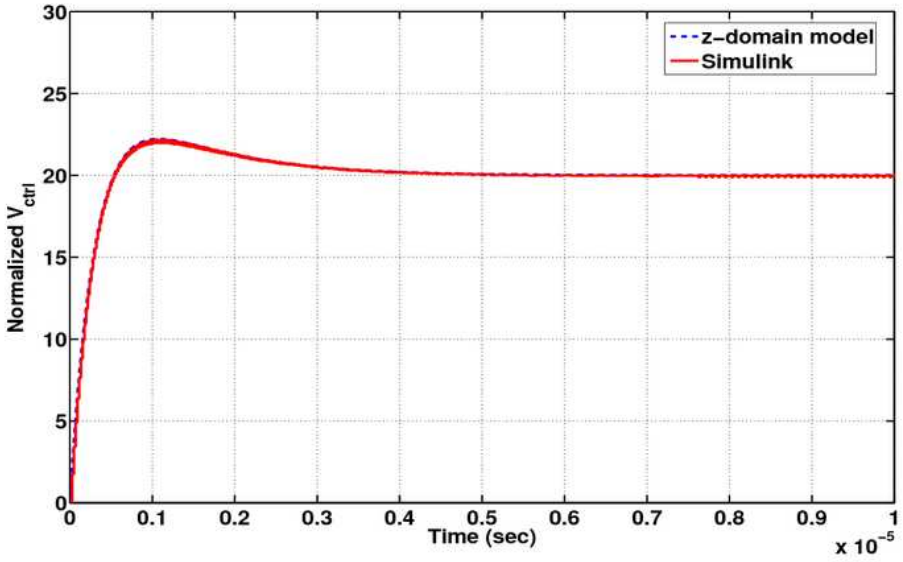


FIGURE 3.18. Response of the digital PLL to a frequency step when it is in lock.

3.5. Radiation Hardening of Digital Phase-Locked Loops

The digital PLL has to be modified to make it tolerant to the effects of radiation. Radiation hardening of the digital PLL involves making it robust to TID and SEE. A method to calibrate the digital PLL on startup and hence making it tolerant to TID has been described in the following section.

3.5.1. Start-up Calibration and TID Hardening

From the analysis of digital phase-locked loops in Section 3.2, the various parameters that influence the performance of a digital PLL are DCAO resolution (f_{LSB}), TDC resolution (dT), update frequency (F_R), proportional gain (α), integral gain (β), normalizing gain (G_n) and the division ratio (N). The DCAO

characteristic is dependent on process variations and temperature and can also be influenced by TID. Similarly, the delay of an inverter is dependent on the environment. The delay can exhibit variations over time, temperature and radiation. The variation of these parameters with the environment influences the performance of a digital PLL. Hence, a calibration scheme is required to counter such variations. A scheme to calibrate digital PLLs against such variations has been described in [15]. The following scheme is a modification of this scheme.

The loop gain of a digital phase-locked loop is expressed as:

$$\frac{\phi_o(z)}{\phi_i(z)} = \frac{1}{N} G_n \frac{T_R}{dT} f_{LSB} T_R \left(\frac{\left(\alpha + \beta - \alpha z^{-1}\right) z^{-1}}{1 - z^{-1}} \right) \tag{3.13}$$

Here, α and β are fixed. The update frequency and the division ratio are also fixed. As a result of variations in dT and f_{LSB}, only the gain quantity preceding the expression gets influenced. For the sake of convenience, let K_{dig} represent this term. Here,

$$K_{dig} = \frac{1}{N} G_n \frac{T_R}{dT} \frac{f_{LSB}}{F_R} \tag{3.14}$$

A variation in K_{dig} as a result of TID would modify the loop bandwidth and the damping of the system. A calibration step would involve keeping K_{dig} independent of the environment. This can be achieved by modifying the normalizing gain G_n to compensate for variations in dT and f_{LSB} and requires the estimation of f_{LSB} and dT.

3.5.2. Estimating the DCAO resolution f_{LSB}

The estimation scheme requires the implementation of a N/N+1 divider. Such a divider can be chosen to divide by N or $N + 1$. First, the PLL would be allowed to lock (sufficient time elapse) for a division ratio N and the control word

output of the digital PLL would be recorded as V_{ctrl}^{N}. After that, the division ratio would be switched to $N+1$. The PLL would be allowed to lock again. The new control word would be recorded as V_{ctrl}^{N+1}. Assuming the DCAO characteristic is relatively linear, the quantity F_R/f_{LSB} can be evaluated as

$$\frac{F_R}{f_{LSB}} = V_{ctrl}^{N+1} - V_{ctrl}^{N} \tag{3.15}$$

3.5.3. Estimating the TDC resolution dT

The period of the DCAO can be measured using the TDC. The period of the DCAO measured using the TDC would give the quantity T_{vco}/dT. We know T_{vco} is equal to T_R/N. This measurement would estimate the value of $\frac{T_R}{NdT}$.

3.5.4. Calibration

For a given nominal value of loopgain K_{dig}^{nom}, the required value of G_n can be estimated as

$$G_n = K_{dig}^{nom} \left\{ \frac{NdT}{T_R} \right\} \left\{ \frac{F_R}{f_{LSB}} \right\} \tag{3.16}$$

The calibration can be used to make the PLL loop parameters independent of the environment. An implementation of this scheme requires digital multipliers and some additional logic circuitry. This scheme has not been implemented on the testchip.

3.6. Single Event Hardening

The effects of single event transients (SET) have been described in Chapter 2. A radiation hardened PLL has to be tolerant to all of those effects. A VCO

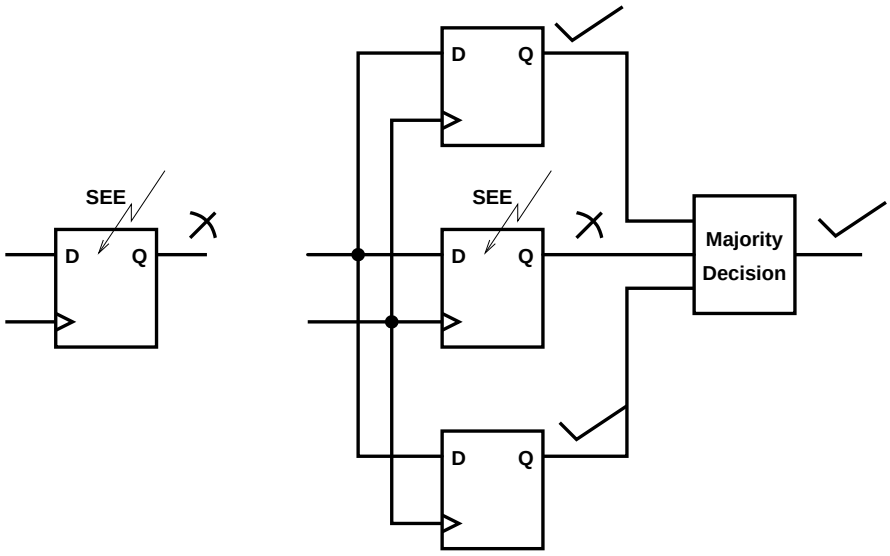
hardened to SET has been described in [16]. This VCO incorporates redundancy in the delay cells to offset the effects of radiation. However, the penalty of a hit on the VCO is less serious compared to the other building blocks of the digital PLL. As described in Chapter 2, the last stages of the frequency divider, the phase detector and the loop filter are the most sensitive blocks in a PLL.

3.6.1. Majority Voting and Redundancy

Digital blocks incorporate redundancy to prevent single event upsets (SEU). Combinational blocks are driven and they are not not seriously effected by SEE. Memory elements in digital systems employ feedback and these elements get corrupted easily during clock transitions. A majority voting relies on the fact that the probability of two adjacent transistors being hit at the same moment is low. It takes at least three elements to make an unambiguous decision when one of the elements is wrong. Fig. 3.19. shows the operation of a majority decision circuit. When such a scheme is not implemented a single latch would suffer as a result of SEU. With redundancy and majority voting, the error in one of the latches is corrected by the other two. This block would replace any latch which is susceptible to SEU.

3.6.2. Frequency Divider

A hit on the first three stages of the frequency divider causes phase errors less than one-eight of the reference cycle. However, these stages account for up to 80% of the power consumption in the frequency divider. Duplication of these blocks doubles the power consumption of the frequency divider. Hence, a trade-off has been made between the power consumption and the severity of the hit.



A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

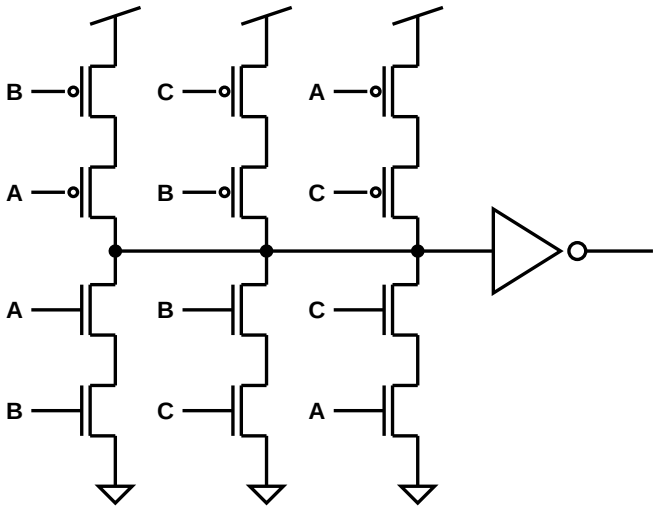


FIGURE 3.19. Majority decision circuit.

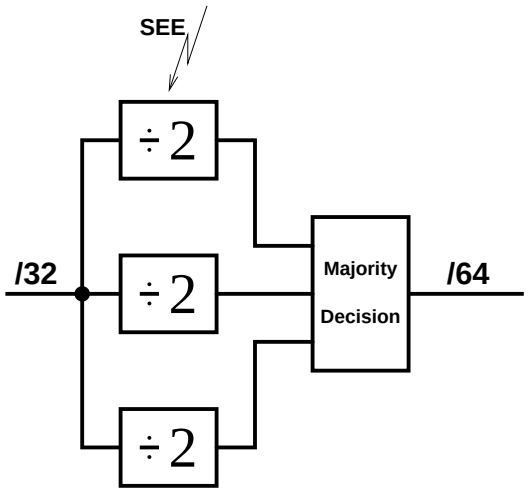


FIGURE 3.20. SEE hardening of a frequency divider.

Thus, only the last three stages of the frequency divider have been made single event tolerant. Fig. 3.20 shows the implementation of redundancy on a frequency divider stage.

3.6.3. Phase/Frequency Detector

The PFD has also been made single event tolerant. The PFD has been replaced by three PFDs. Two majority decision circuits were implemented to generate the correct UP and DN pulses. Fig. 3.21 shows the implementation of redundancy on the PFD.

3.6.4. Time-to-Digital Converter

A single event strike on any of the latches in the TDC can cause an error in the latch values. The penalty of a bit flip in the LSBs is low. However, a bit flip in the MSBs of the TDC can cause an error transient. This error transient can cause

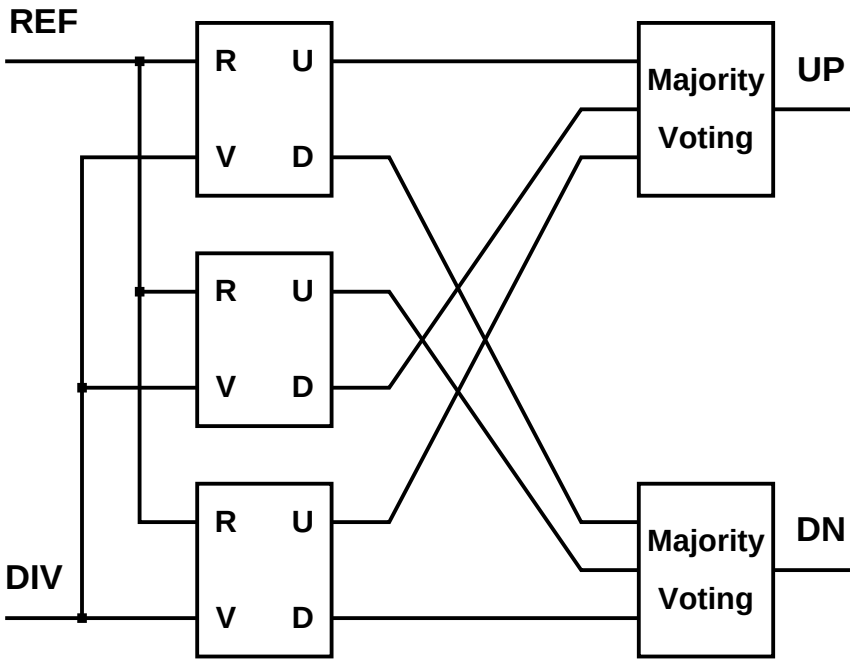


FIGURE 3.21. Implementation of redundancy and majority voting for the PFD.

the PLL to lose phase lock and requires several micro seconds to restore phase lock. These latches were duplicated and majority voting implemented to prevent single event upsets. The LSBs of the digital PLL are active during the tracking phase. Duplicating these latches would increase the power consumption of the TDC drastically. To prevent this, a trade off has been made between penalty of an error and power consumption. Only the seven MSBs of the TDC were made single event tolerant. This case keeps the power consumption low and also prevent the loss of phase lock. Fig. 3.22 shows the implementation of redundancy and majority voting in a TDC. It can also be seen that the sign bit of the TDC is protected from SEE.

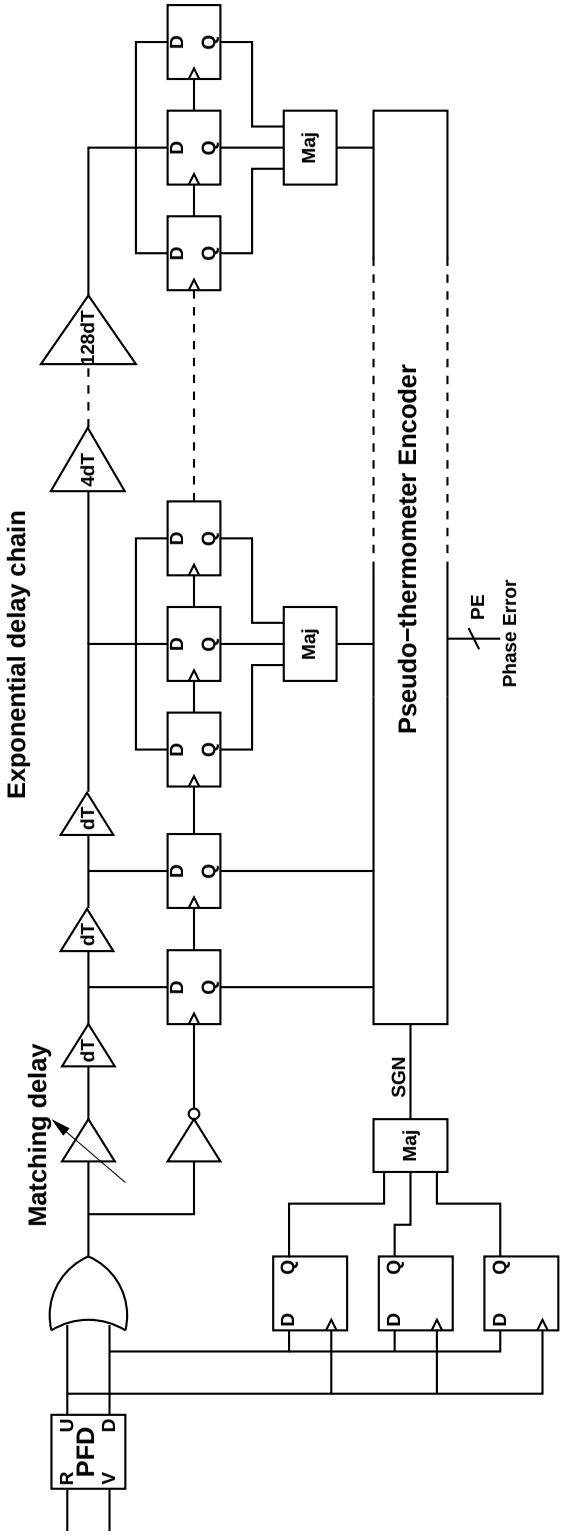


FIGURE 3.22. Implementation of redundancy and majority voting on the TDC.

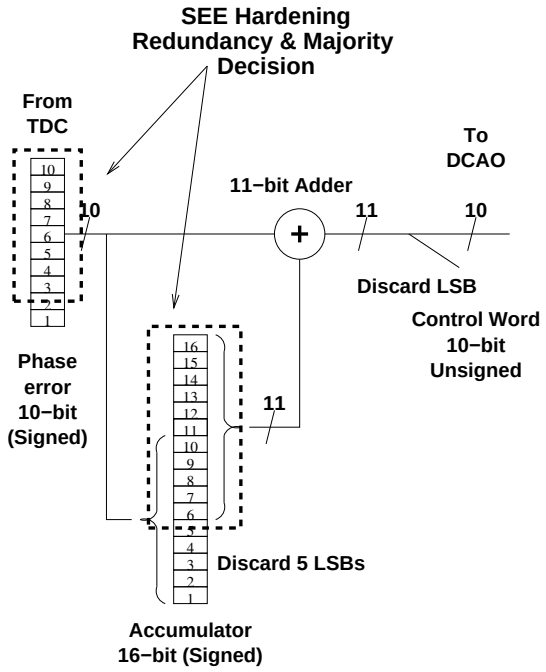


FIGURE 3.23. SEE hardening of the TDC and loop filter.

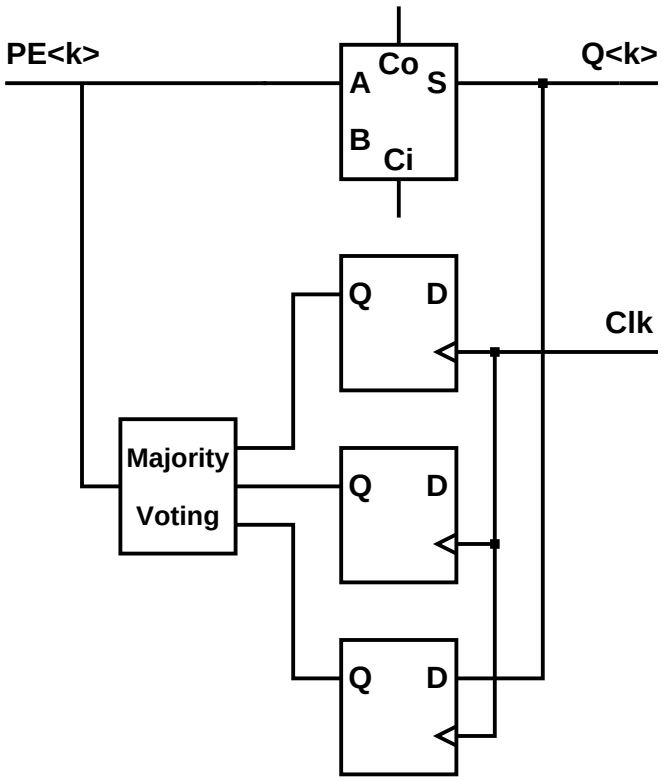


FIGURE 3.24. SEE hardening of a single bit of accumulator.

3.6.5. Digital Loop Filter

The accumulator on the digital loop filter is the most susceptible block in a digital PLL. Any SEE in the MSBs of the accumulator can cause the PLL to lose lock. In order to prevent this, the 11 MSBs of the accumulator were protected using redundancy and majority voting. Fig. 3.23 shows the radiation hardening of the TDC and loop filter by duplicating the susceptible and sensitive latches. The latches enclosed in the dashed box have been protected. Fig. 3.24 shows the radiation hardening of a single bit of accumulator by duplicating the latches and implementing majority voting.

3.7. Layout of the Test Chip

The layout of the testchip is shown in Fig. 3.25. This chip has been fabricated in Honeywell 0.35μm SOI CMOS process.

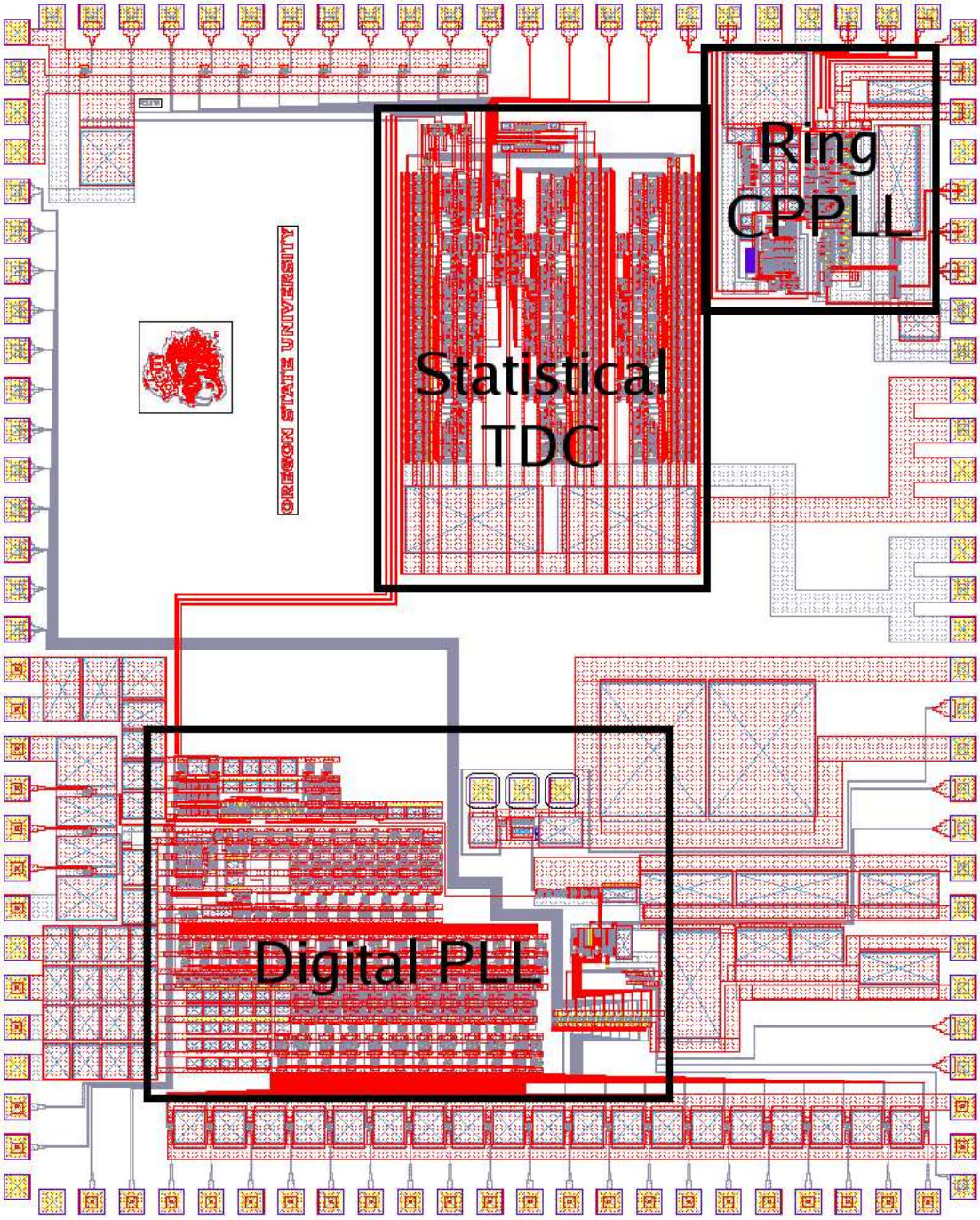


FIGURE 3.25. Layout of the test chip.

4. SUMMARY AND CONCLUSIONS

The objective of this project was to develop radiation hardened phase-locked loops. As a part of this project, the effects of radiation on PLLs and its various building blocks have been studied. These studies provided the required information about the effects of radiation in phase-locked loops. This information was used to design a radiation hardened digital phase-locked loop. The following points summarize the main points of this project:

- Total ionization dose usually increases the threshold voltage of PMOS transistors and reduces the threshold voltage of NMOS transistors.
- Total ionization dose also enhances the gate leakage current.
- The shift in threshold voltages might eventually prevent the NMOS transistors from switching off and PMOS transistors from switching on. This would culminate in functional failure of a circuit.
- Digital circuits are less sensitive to variations in threshold voltages as opposed to analog circuits. As a consequence, the effects of TID on digital circuits are less serious than in analog circuits.
- Exposure of a PLL to radiation results in the shift of VCO tuning characteristics and the charge pump bias currents. This variation in loop parameters of the PLL leads to a change in the loop bandwidth and the damping factors. This could lead to peaking in the jitter transfer function.
- The PLL loop characteristics can be made independent of the environment through calibration. Analog calibration circuits themselves are susceptible to TID. Hence, digital loop calibration techniques have to be employed.

- Single event transients are created as a result of a high energy particle hitting an active device. Such transients cause jitter in VCOs.

- These transients are less serious in static blocks and more serious in latches and comparators. Latches and comparators employ positive feedback to enhance settling times. Error transients during this phase can lead to incorrect decisions.

- Single event transients in the last stages of the frequency divider, phase detector and the loop filter are most serious. A hit on any of those blocks can result in the loss of phase lock. Restoration of lock requires several microseconds. This could corrupt a data stream being transmitted or received in a communication system. A microprocessor employing such a PLL for a clock would not function correctly during that period.

- Single event effects in frequency dividers and phase detectors can be prevented through the employment of redundancy and majority voting. But, the loop filter in a conventional PLL cannot be protected from single event upsets.

- An all digital phase-locked loop employs only digital gates and digital latches. All its blocks can be protected from SEE through redundancy and majority voting. A digital phase-locked loop can also employ digital calibration techniques to counter the effects of TID.

- A digital phase locked loop with redundancy and majority voting has been designed and taped out in a 0.35μm SOI CMOS technology.

- This PLL does not incorporate the suggested startup calibration circuitry. Implementing this calibration circuitry would make this PLL a fully radiation hardened phase-locked loop.

- The analysis presented in this report assumes a linear operation of the phase detector. This analysis predicts the acquisition of lock accurately. However, the non-linear nature of the phase detector has to be accounted for in order to study the jitter suppression in digital phase locked loops.

- The test chip has to be measured and characterized to test its operation and performance. Exposing this PLL to single event testing would validate the primary claims of this project.

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